



# RF Power Field Effect Transistors

## N-Channel Enhancement-Mode Lateral MOSFETs

Designed for CDMA base station applications with frequencies from 1930 to 1990 MHz. Suitable for CDMA and multicarrier amplifier applications. To be used in Class AB and Class C for PCN-PCS/cellular radio and WLL applications.

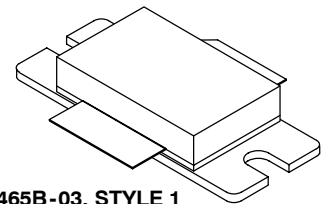
- Typical Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Volts,  $I_{DQ} = 1400$  mA,  $P_{out} = 50$  Watts Avg., Full Frequency Band, 3GPP Test Model 1, 64 DPCH with 50% Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.  
 Power Gain — 17.2 dB  
 Drain Efficiency — 32%  
 Device Output Signal PAR — 6.2 dB @ 0.01% Probability on CCDF  
 ACPR @ 5 MHz Offset — -37.5 dBc in 3.84 MHz Channel Bandwidth
- Capable of Handling 5:1 VSWR, @ 32 Vdc, 1960 MHz, 170 Watts CW Peak Tuned Output Power
- $P_{out}$  @ 1 dB Compression Point  $\geq 170$  Watts CW

### Features

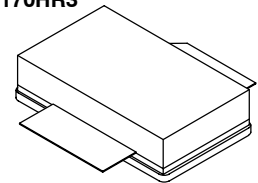
- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

**MRF7S19170HR3**  
**MRF7S19170HSR3**

**1930-1990 MHz, 50 W AVG., 28 V**  
**SINGLE W-CDMA**  
**LATERAL N-CHANNEL**  
**RF POWER MOSFETs**



**CASE 465B-03, STYLE 1**  
**NI-880**  
**MRF7S19170HR3**



**CASE 465C-02, STYLE 1**  
**NI-880S**  
**MRF7S19170HSR3**

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	-6.0, +10	Vdc
Operating Voltage	$V_{DD}$	32, +0	Vdc
Storage Temperature Range	$T_{stg}$	- 65 to +150	°C
Case Operating Temperature	$T_C$	150	°C
Operating Junction Temperature (1,2)	$T_J$	225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
Case Temperature 80°C, 170 W CW		0.25	
Case Temperature 72°C, 25 W CW		0.31	

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	1A (Minimum)
Machine Model (per EIA/JESD22-A115)	B (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

**Table 4. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Off Characteristics**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 372\ \mu\text{Adc}$ )	$V_{GS(th)}$	1.2	2	2.7	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28\text{ Vdc}$ , $I_D = 1400\text{ mAdc}$ )	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage (1) ( $V_{DS} = 28\text{ Vdc}$ , $I_D = 1400\text{ mAdc}$ , Measured in Functional Test)	$V_{GG(Q)}$	4	5.4	7.6	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 3.72\text{ Adc}$ )	$V_{DS(on)}$	0.1	0.15	0.3	Vdc

**Dynamic Characteristics (2)**

Reverse Transfer Capacitance ( $V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{rss}$	—	0.9	—	pF
Output Capacitance ( $V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{oss}$	—	703	—	pF

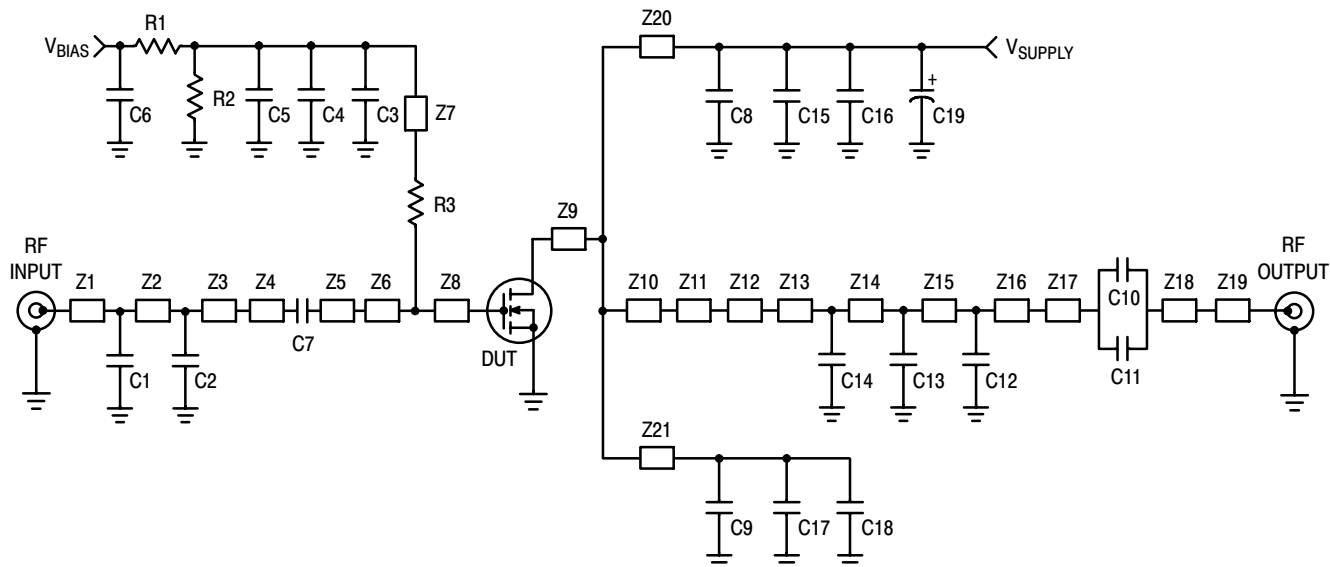
**Functional Tests** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ} = 1400\text{ mA}$ ,  $P_{out} = 50\text{ W Avg.}$ ,  $f = 1932.5\text{ MHz}$  and  $f = 1987.5\text{ MHz}$ , Single-Carrier W-CDMA, 3GPP Test Model 1, 64 DPCH, 50% Clipping, PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5\text{ MHz}$  Offset.

Power Gain	$G_{ps}$	16	17.2	19	dB
Drain Efficiency	$\eta_D$	29	32	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	5.7	6.2	—	dB
Adjacent Channel Power Ratio	ACPR	—	-37.5	-35	dBc
Input Return Loss	IRL	—	-16	-9	dB

- $V_{GG} = 2 \times V_{GS(Q)}$ . Parameter measured on Freescale Test Fixture, due to resistive divider network on the board. Refer to Test Circuit schematic.
- Part internally matched both on input and output.

**Table 4. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted) — continued

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Typical Performances</b> (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$ , $I_{DQ} = 1400\text{ mA}$ , 1930-1990 MHz Bandwidth					
Video Bandwidth (Tone Spacing from 100 kHz to VBW) $\Delta\text{IMD3} = \text{IMD3 @ VBW frequency} - \text{IMD3 @ 100 kHz} < 1\text{ dBc}$ (both sidebands)	VBW	—	25	—	MHz
Gain Flatness in 60 MHz Bandwidth @ $P_{\text{out}} = 170\text{ W CW}$	$G_F$	—	0.5	—	dB
Deviation from Linear Phase in 60 MHz Bandwidth @ $P_{\text{out}} = 170\text{ W CW}$	$\Phi$	—	2.06	—	°
Group Delay @ $P_{\text{out}} = 170\text{ W CW}$ , $f = 1960\text{ MHz}$	Delay	—	4.7	—	ns
Part-to-Part Insertion Phase Variation @ $P_{\text{out}} = 170\text{ W CW}$ , $f = 1960\text{ MHz}$	$\Delta\Phi$	—	16	—	°
Gain Variation over Temperature	$\Delta G$	—	0.015	—	dB/°C
Output Power Variation over Temperature	$\Delta P_{1\text{dB}}$	—	0.01	—	dBm/°C



Z1*	0.588" x 0.083" Microstrip	Z12	0.060" x 0.420" Microstrip
Z2*	0.146" x 0.083" Microstrip	Z13*	0.197" x 0.083" Microstrip
Z3*	0.068" x 0.083" Microstrip	Z14*	0.332" x 0.083" Microstrip
Z4	0.865" x 0.098" Microstrip	Z15*	0.158" x 0.083" Microstrip
Z5	0.154" x 0.098" Microstrip	Z16*	0.572" x 0.083" Microstrip
Z6	0.271" x 0.787" Microstrip	Z17, Z18	0.063" x 0.220" Microstrip
Z7	1.410" x 0.080" Microstrip	Z19	0.160" x 0.083" Microstrip
Z8	0.194" x 0.787" Microstrip	Z20, Z21	1.120" x 0.080" Microstrip
Z9	0.115" x 1.360" Microstrip	PCB	Taconic TLX-0300, 0.030", $\epsilon_r = 2.5$
Z10	0.230" x 1.360" Microstrip		
Z11	0.185" x 1.120" Microstrip		

\* Variable for tuning

Figure 1. MRF7S19170HR3(HSR3) Test Circuit Schematic

Table 5. MRF7S19170HR3(HSR3) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2	1.8 pF Chip Capacitors	100B1R8BW	ATC
C3, C8, C9, C10, C11	8.2 pF Chip Capacitors	100B8R2CW	ATC
C4	100 pF Chip Capacitor	100B101JW	ATC
C5	100 nF Chip Capacitor	200B104MW	ATC
C6, C15, C16, C17, C18	10 $\mu$ F Chip Capacitors	C5750X5R1H106MT	TDK
C7	0.5 pF Chip Capacitor	100B0R5BW	ATC
C12	1.5 pF Chip Capacitor	100B1R5BW	ATC
C13	0.3 pF Chip Capacitor	100B0R3BW	ATC
C14	0.8 pF Chip Capacitor	100B0R8BW	ATC
C19	470 $\mu$ F, 63 V Electrolytic Capacitor, Axial	516D477M063PS7B	Sprague
R1, R2	10 k $\Omega$ , 1/4 W Chip Resistors	CRCW12061001FKTA	Vishay
R3	10 $\Omega$ , 1/4 W Chip Resistor	CRCW120610R0FKTA	Vishay

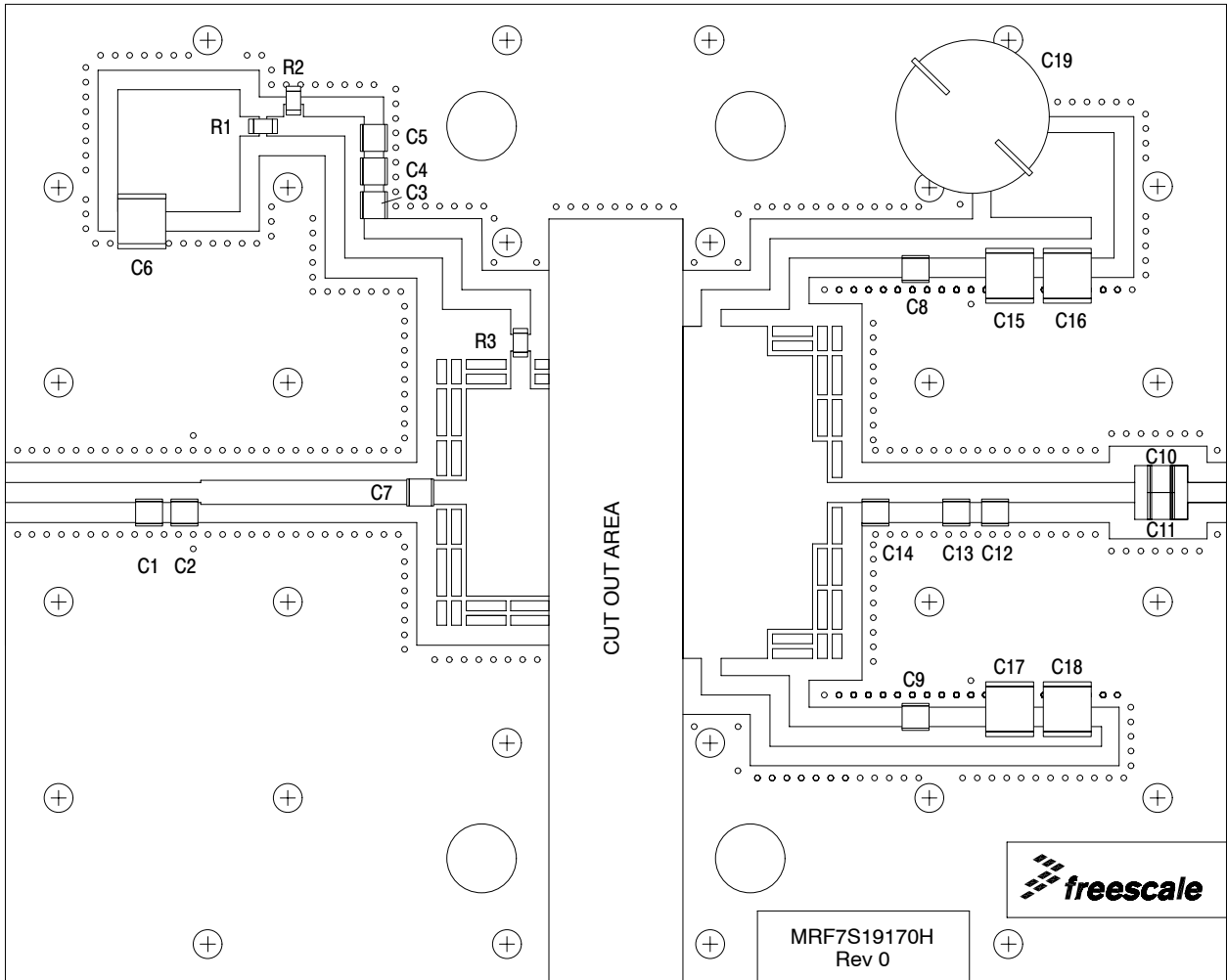
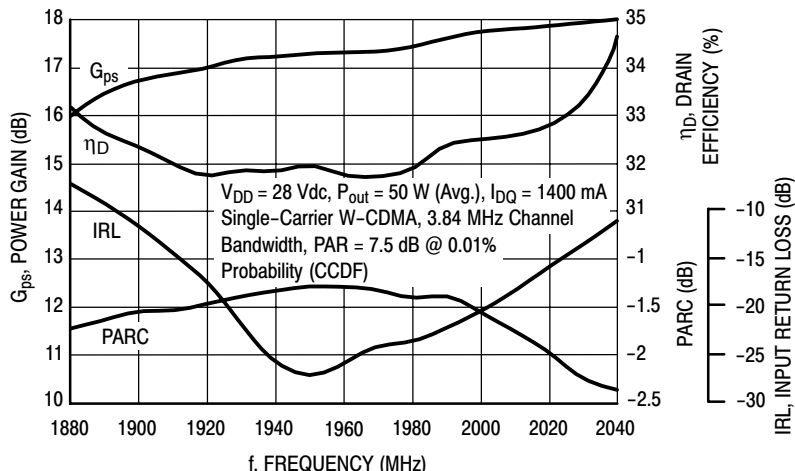
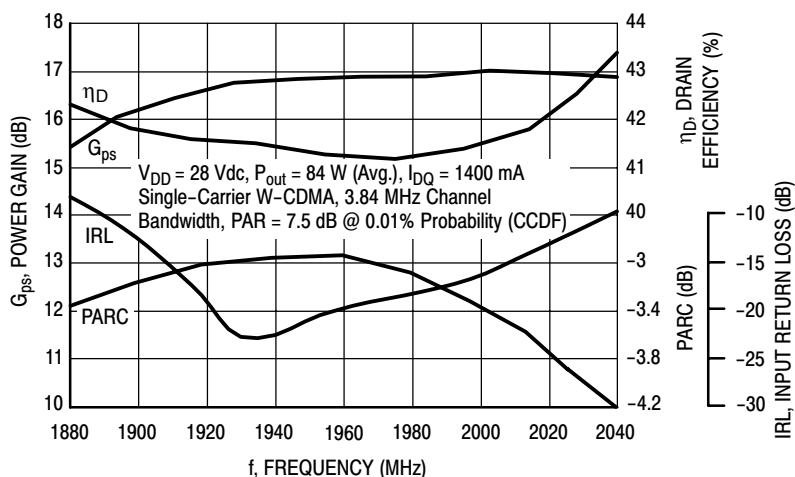


Figure 2. MRF7S19170HR3(HSR3) Test Circuit Component Layout

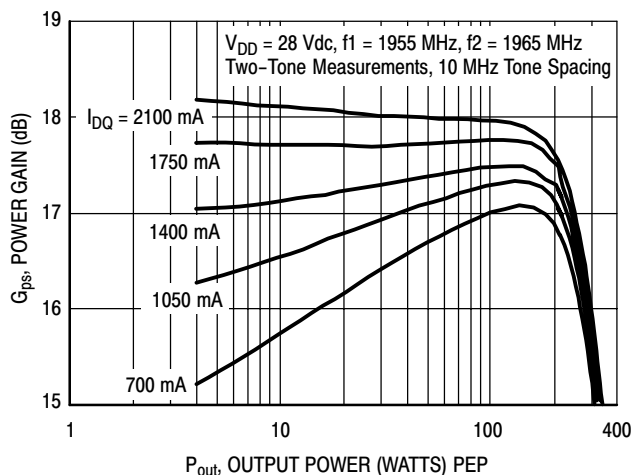
## TYPICAL CHARACTERISTICS



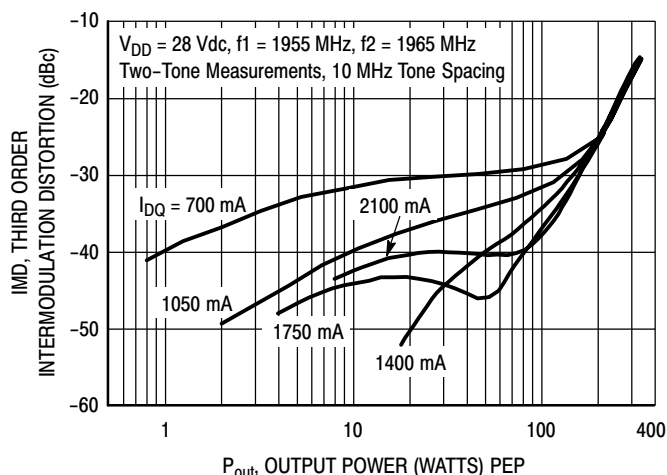
**Figure 3. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 50$  Watts Avg.**



**Figure 4. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 84$  Watts Avg.**

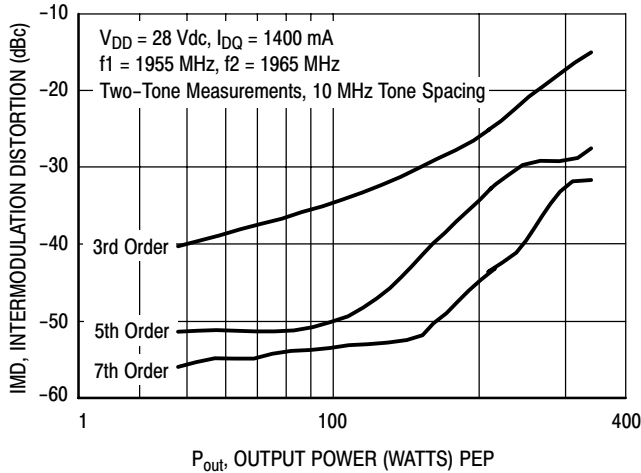


**Figure 5. Two-Tone Power Gain versus Output Power**

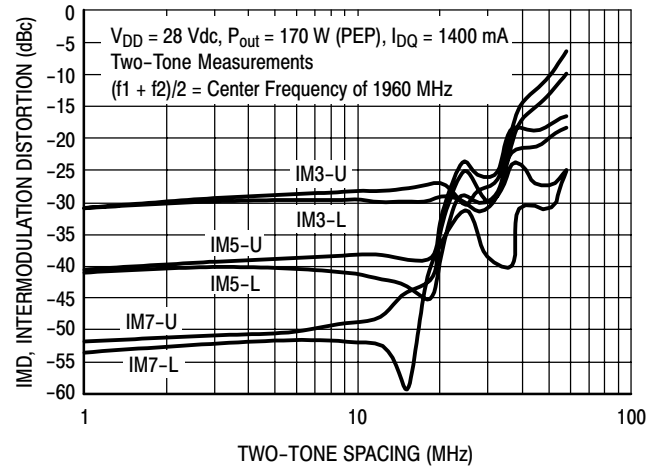


**Figure 6. Third Order Intermodulation Distortion versus Output Power**

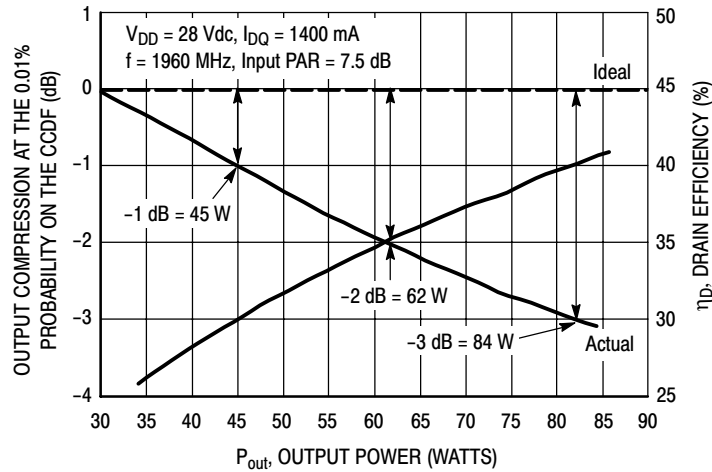
## TYPICAL CHARACTERISTICS



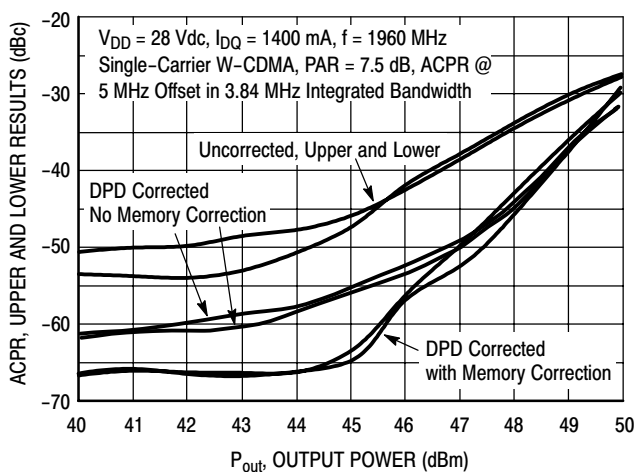
**Figure 7. Intermodulation Distortion Products versus Output Power**



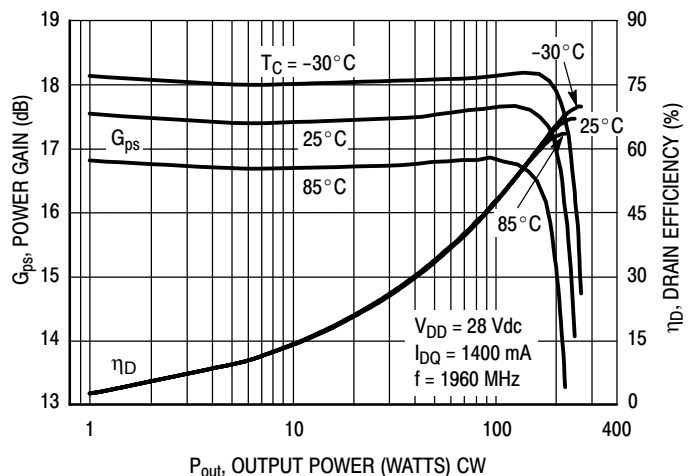
**Figure 8. Intermodulation Distortion Products versus Tone Spacing**



**Figure 9. Output Peak-to-Average Ratio Compression (PARC) versus Output Power**



**Figure 10. Digital Predistortion Correction versus ACPR and Output Power**



**Figure 11. Power Gain and Drain Efficiency versus CW Output Power**

MRF7S19170HR3 MRF7S19170HSR3

## TYPICAL CHARACTERISTICS

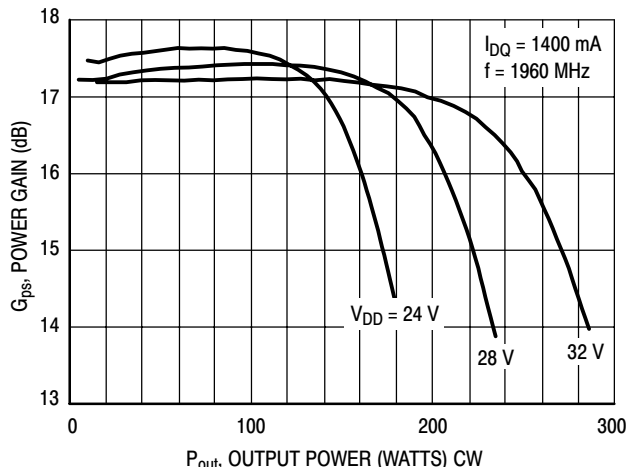
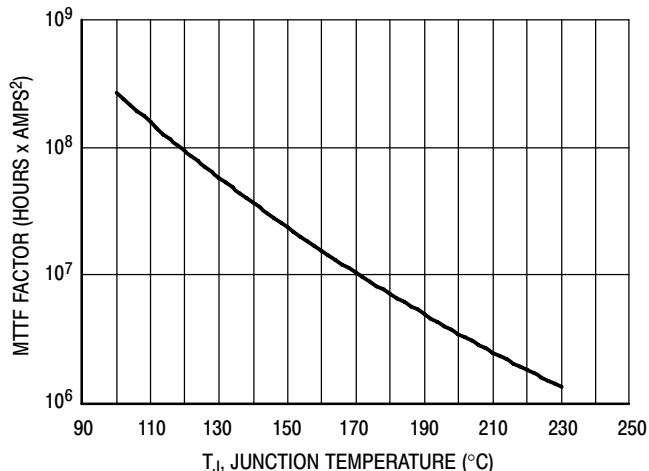


Figure 12. Power Gain versus Output Power



This above graph displays calculated MTTF in hours x ampere<sup>2</sup> drain current. Life tests at elevated temperatures have correlated to better than  $\pm 10\%$  of the theoretical prediction for metal failure. Divide MTTF factor by  $I_D^2$  for MTTF in a particular application.

Figure 13. MTTF Factor versus Junction Temperature

## W-CDMA TEST SIGNAL

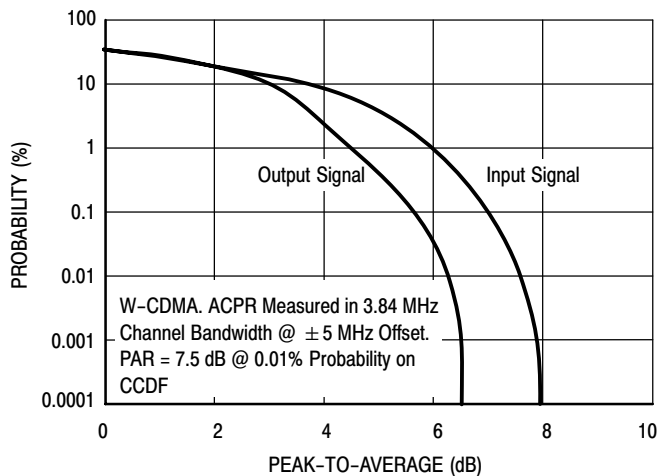


Figure 14. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 50% Clipping, Single-Carrier Test Signal

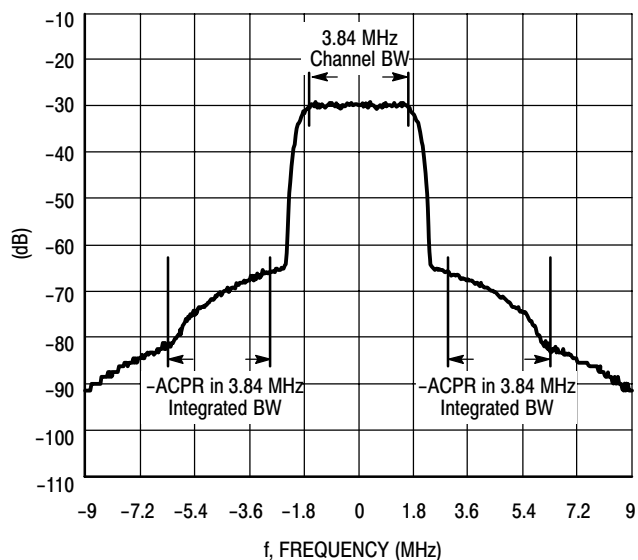
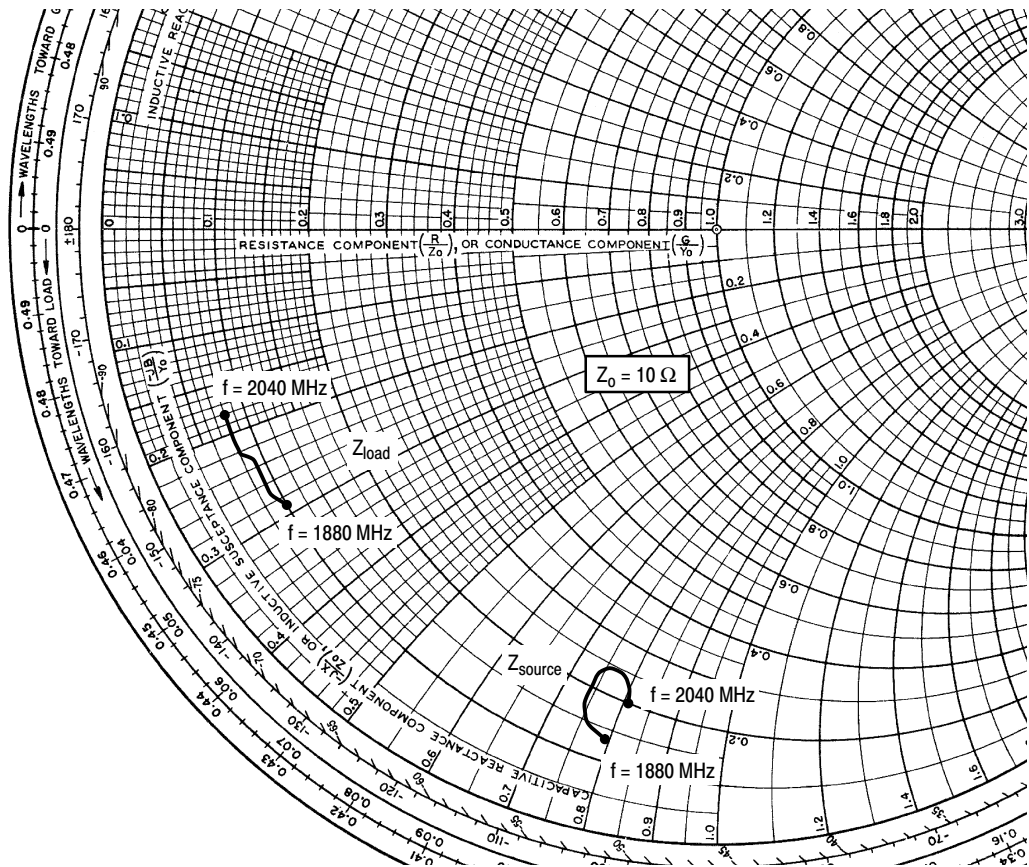


Figure 15. Single-Carrier W-CDMA Spectrum





$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 1400 \text{ mA}$ ,  $P_{out} = 50 \text{ W CW Avg.}$

f MHz	Z <sub>source</sub> Ω	Z <sub>load</sub> Ω
1880	1.338 - j7.859	0.967 - j2.868
1900	1.515 - j7.609	0.942 - j2.725
1920	1.743 - j7.432	0.920 - j2.585
1940	2.007 - j7.352	0.893 - j2.449
1960	2.249 - j7.393	0.865 - j2.313
1980	2.410 - j7.553	0.841 - j2.192
2000	2.411 - j7.788	0.820 - j2.073
2020	2.244 - j7.995	0.802 - j1.957
2040	1.966 - j8.101	0.779 - j1.834

Z<sub>source</sub> = Test circuit impedance as measured from gate to ground.

Z<sub>load</sub> = Test circuit impedance as measured from drain to ground.

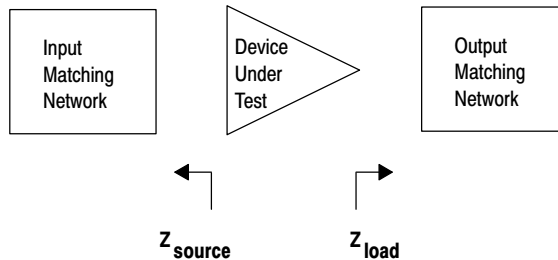
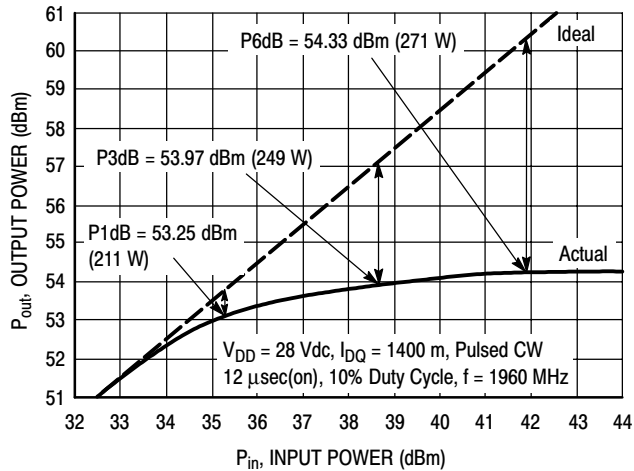


Figure 16. Series Equivalent Source and Load Impedance

## ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS

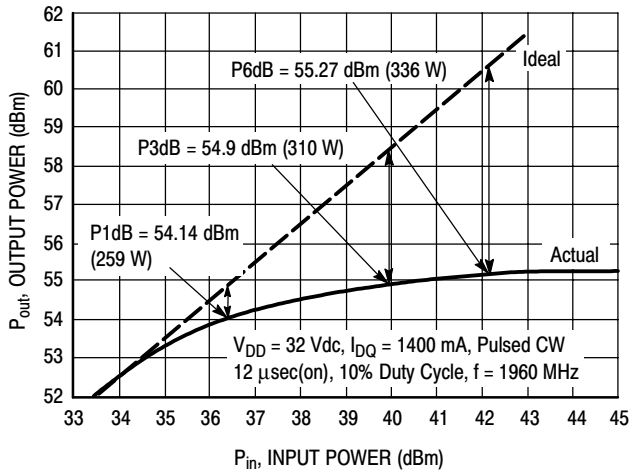


NOTE: Measured in a Peak Tuned Load Pull Fixture

Test Impedances per Compression Level

	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
P3dB	2.34 - j9.24	0.79 - j2.94

**Figure 17. Pulsed CW Output Power versus Input Power**



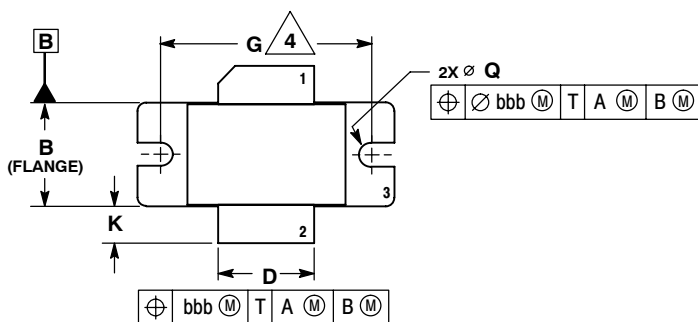
NOTE: Measured in a Peak Tuned Load Pull Fixture

Test Impedances per Compression Level

	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
P3dB	2.34 - j9.24	0.79 - j2.94

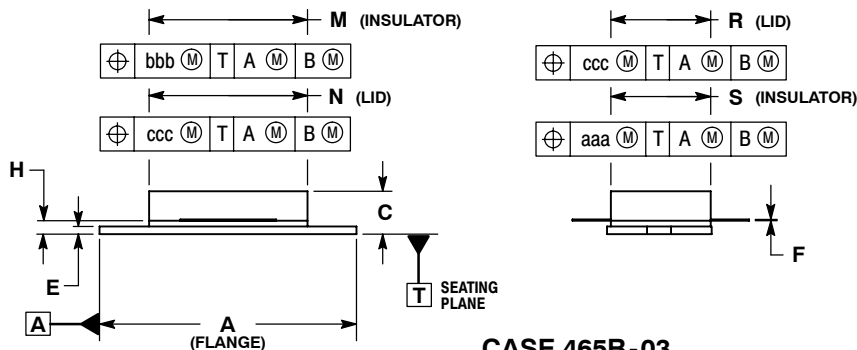
**Figure 18. Pulsed CW Output Power versus Input Power**

## PACKAGE DIMENSIONS



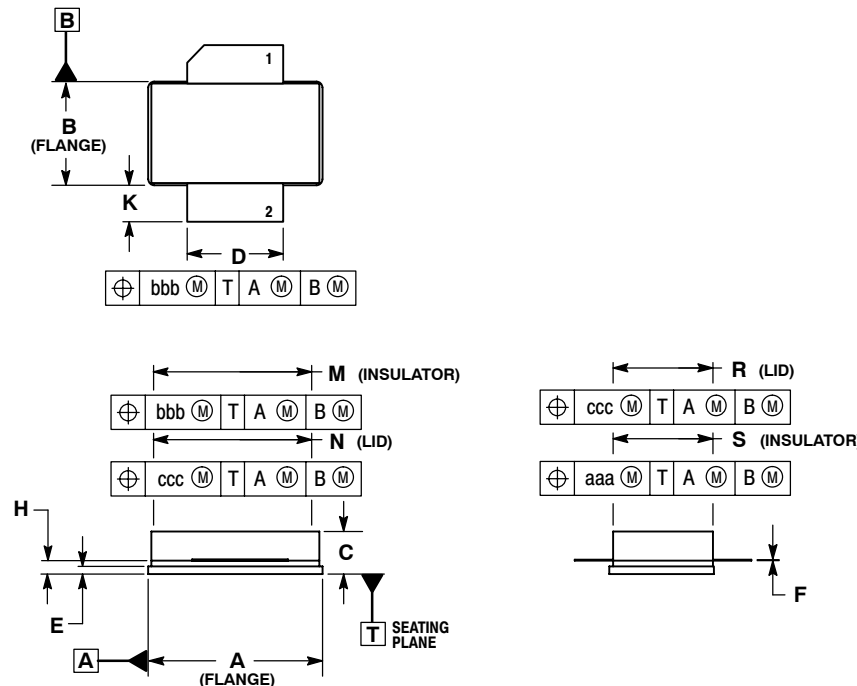
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
  4. RECOMMENDED BOLT CENTER DIMENSION OF 1.16 (29.57) BASED ON M3 SCREW.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.535	0.545	13.6	13.8
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.175	0.205	4.44	5.21
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
Q	∅.118	∅.138	∅3.00	∅3.51
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	



- STYLE 1:  
 PIN 1. DRAIN  
 2. GATE  
 3. SOURCE

**CASE 465B-03  
 ISSUE D  
 NI-880  
 MRF7S19170H**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.905	0.915	22.99	23.24
B	0.535	0.545	13.60	13.80
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

- STYLE 1:  
 PIN 1. DRAIN  
 2. GATE  
 3. SOURCE

**CASE 465C-02  
 ISSUE D  
 NI-880S  
 MRF7S19170HS**

**MRF7S19170HR3 MRF7S19170HSR3**

## PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

### Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Oct. 2006	<ul style="list-style-type: none"><li>• Initial Release of Data Sheet</li></ul>

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